Docket No: 40291/2000100

In the Specification:

On page 2 (page 2 begins the "Background of the Invention" section), after line 2 and before the first paragraph, please add the following subsection heading (i.e., the "Field of the Invention" is a subsection of the "Background of the Invention" section):

"**Field of the Invention**"

On page 2, after line 8 and before the second paragraph, please add the following subsection heading:

"**Background Information**"

On page 2, please delete line 20 (i.e., please delete the words "Figure 1").

On page 2, line 21, please delete Figure 1 entitled "Network Processor in a Line Card".

On page 3, please delete line 20 (i.e., please delete the words "Figure 2").

On page 3, line 21, please delete Figure 2 entitled "Moore's Law Vs Bandwidth Demand".

On page 5, please delete line 1 (i.e., please delete the words "Figure 3").

On page 5, line 2, please delete Figure 3 entitled "Memory Hierarchy in a Computer System".

On page 5, after the second paragraph that begins with "Caching theory works well...." and before the "Summary of the Invention" section, please add the following new paragraph:

A1

Therefore, it is desirable to have a system and method to efficiently access a memory unit while processing network traffic.

On page 6, please delete line 12 (i.e., please delete the words "Figure 4").

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On page 6, line 13, please delete Figure 4 entitled "Memory Management Subsystems".

On page 8, after line 5, please add the following section and the brief descriptions of the figures:

Brief Description of the Drawings

Figure 1 illustrates a prior art line card and its components.

Figure 2 illustrates Moore's Law versus the Internet bandwidth demand curve.

Figure 3 illustrates a prior art multilevel memory hierarchy within a processor.

Figure 4 illustrates an embodiment of a memory management subsystem according to the present invention.

Figure 5 illustrates an embodiment of a network processor according to the present invention.

Figure 6 illustrates an embodiment of a payload channel sequence table according to the present invention.

Figure 7 illustrates an embodiment of a bandwidth balancing flowchart according to the present invention.

On page 10, please delete line 7 (i.e., please delete the words "Figure 5").

On page 10, line 8, please delete Figure 5 entitled "Bandwidth Balancer Data Structure".

On page 12, please delete line 5 (i.e., please delete the words "Figure 6").

On page 12, line 6, please delete Figure 6 entitled "Payload Channel Sequence Table Structure".

On page 14, please delete line 1 (i.e., please delete the words "Figure 7").

On page 14, line 2, please delete Figure 7 entitled "Bandwidth Balancing Algorithm Flow Chart".